REMARKS

Claims 1-17, 20 and 21 are pending in this application, of which claims 11-17 have been withdrawn from consideration and claims 18 and 19 have been canceled. Claims 20 and 21 have been newly added. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Rejections under 35 U.S.C. §103

Claims 1, 2, 5 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over K. Kasai et al. (*W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs*) in view of Jeng et al. (U.S. Patent No. 5,877,074).

Applicants respectfully traverse this rejection.

The Examiner alleged that Kasai et al and Jeng et al disclose the semiconductor device having two polycrystalline silicon layers comprising a discontinuous grain boundary, and since Jeng et al teaches the thickness of the second polycrystalline silicon film 32 that includes the claimed range, the combination of the references clearly renders claims 1, 2, 5 and 6 obvious.

However, claims 1, 2, 5 and 6 recite, among other things, "a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness of 2-20 nm and thinner than that of the first polycrystalline silicon film and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film." The thickness of the amorphous silicon film of Kasai et al cannot be made as thin as the second polycrystalline silicon film of the claimed invention.

In the present invention, the thickness of the second polycrystalline silicon film is set to 2-20 nm. Due to this feature of the present invention, the dopant diffusion from the first polycrystalline silicon film to the metal nitride film formed on the second polycrystalline silicon film can be suppressed without increasing the contact resistance. That is, when the thickness of the second polycrystalline silicon film is thinner than 2 nm, all the polycrystalline silicon film reacts with the metal nitride film and the dopant diffusion cannot be suppressed. When the thickness of the second polycrystalline silicon film is thicker than 20 nm, supply of the dopant impurity from the first polycrystalline silicon film to the second polycrystalline silicon film is insufficient and the contact resistance between the second polycrystalline silicon film and the metal nitride film increases.

The native oxide film or the chemical oxide film is formed between the first polycrystalline silicon film and the second polycrystalline silicon film, whereby the dopant diffusion can be effectively suppressed.

As the result of suppressing the dopant diffusion by the interface between the first polycrystalline silicon film and the second polycrystalline silicon film, the dopant concentration in the first polycrystalline silicon film near the interface between the first polycrystalline silicon film and the second polycrystalline silicon film becomes higher than the dopant concentration in the second polycrystalline silicon film near the interface between the first polycrystalline silicon film and the second polycrystalline silicon film.

On the other hand, in Kasai et al, the amorphous silicon film is formed in order to fabricate the dual gate CMOS structure including n^+ polycrystalline silicon gate for the n-type transistors and the p^+ polycrystalline silicon gate for the p-type transistors. The amorphous silicon film is formed in order to suppress impurity diffusion between the n^+ and the p^+ polycrystalline silicon (mutual diffusion of the

impurities) during the fabrication process (see page 19.4.1, right column, lines 20-22). Thus, it is thought that the thickness of the amorphous silicon film is set as 100 nm in order to suppress mutual diffusion of impurities.

In Kasai et al, doping to the first polycrystalline silicon film and amorphous silicon film are conducted after the formation of these films so as to form dual gate CMOS structure. Thus, the amorphous silicon film also functions as a channeling stopper for suppressing the penetration of the implanted ions through the first polycrystalline silicon film to the substrate. Based on this, the amorphous silicon film cannot be made thin. As described in Kasai et al, when the dual gate doping is carried out by P^+ implantation at 30 keV and B^+ implantation at 15 keV (see page 9.4.1, right column lines 22-24), the projected ranges of the implanted P^+ ions and B^+ ions are about 40 nm and 50 nm, respectively. When the thickness of the amorphous silicon film is set to less than about 40 nm, the projected ranges are positioned in the first polycrystalline silicon film, so that the penetration of the implanted ions to the substrate cannot be suppressed by the amorphous silicon film. Kasai et al neither teaches nor suggests making the thickness of the amorphous silicon film thin.

Thus, the thickness of the amorphous silicon film of Kasai et al cannot be made as thin as the thickness of the second polycrystalline silicon film of the claimed invention.

The Examiner also alleged that Jeng et al teaches the thickness of the second polycrystalline silicon film 32 that includes the claimed range. However, this disclosure of Jeng et al would not provide any motivation for setting the thickness of the amorphous silicon film of Kasai et al to 20-40 nm.

In Jeng et al, the amorphous silicon film 32 is formed between the polycrystalline silicon film 31 and the tungsten silicide film 14 in order to prevent the peeling of the tungsten silicide film 14 and the diffusion of the fluorine introduced from WF_6 gas during the deposition of the tungsten silicide film 14. In Jeng et al, paying attention to the effects that the doped polycrystalline silicon is easier for fluorine atoms to diffuse through than undoped polycrystalline silicon and the undoped polycrystalline is easier for fluorine atoms to diffuse through than amorphous silicon, the undoped amorphous silicon film is formed over the first polycrystalline silicon film. When the thickness of the amorphous silicon film is too thick, the contact resistance between the first polycrystalline silicon film and the tungsten silicide film increases. When the thickness of the amorphous silicon flim is too thin, the effect of preventing the fluorine diffusion is lowered. Thus, in Jeng et al, the thickness of the amorphous silicon film is set to 20-40 nm. Contrary to Kasai et al, in Jeng et al, the thickness of the amorphous silicon film can be set to such thickness because the first polycrystalline silicon film is deposited in the doped state. It is not necessary for Jeng et al to take into account the mutual diffusion of the impurities, since the n^+ polycrystalline silicon film is used in both of the n-type transistors and the p-type transistors.

As described above, the thickness of the amorphous silicon film to be the second polycrystalline silicon film of Kasai et al and that of Jeng et al are set based on the respective objects which are different from each other. Thus, this disclosure would not provide any motivation for setting the thickness of the amorphous silicon film of Kasai et al to 20-40 nm.

For at least these reasons, claims 1, 2, 5 and 6 patentably distinguish over Kasai et al. and Jeng et al., and the 35 U.S.C. §103(a) rejection should be withdrawn.

Claims 3, 4 and 7-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kasai et al. and Jeng et al., and further in view of Tsukamoto (U.S. 2001/0000629Al).

Applicants respectfully traverse this rejection.

The Examiner alleged that Kasai et al. and Jeng et al. were shown to teach all the features of the claims with the exception of explicitly disclosing an oxide film formed between the first and second polycrystalline silicon films, and that Tsukamoto teaches a native oxide film 20 is formed between the first 6 and second 7 polycrystalline silicon films so that the grain size of the second polycrystalline silicon film 7 can become large. Based on these disclosures, the Examiner concluded that it would have been obvious to one having ordinary skill in the art at the time of invention to form an oxide film between the first and second polycrystalline silicon films of Kasai et al. as taught by Tsukamoto to suppress fluctuation in the threshold voltage V_{th}.

However, such disclosures of Tsukamoto do not remedy the deficiencies of Kasai et al. and Jeng et al. For at least these reasons, claims 3, 4 and 7-10, depending from claims 1 and 2, patentably distinguish over Kasai et al., Jeng et al. and Tsukamoto.

Thus, the 35 U.S.C. §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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